



EPI Europe strikes back on HPC (*)

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(*) to Top500

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EPI - Europe's Ambition

- Design a roadmap of future European low power processors targeting
 - Extreme scale computing,
 - High performance big data, and
 - Emerging applications
- FPA answering EU Horizon 2020 (FP8) ICT-42-2017 call

* FPA : Framework Partnership Agreement

* FP8 : Framework Programmes 8 for 2014-2020, succeeding FP7 (2007-2013)

EPI Mission

- European Independence in High Performance Computing Processor Technologies
 - Goal: EU ExaScale machines based on EU processor by 2023
 - Tentatively, one pre-ExaScale machine in 2021 with Gen1 processor (RHEA)

AND

- Based on a **solid**, **long-term economic model**
 - Go beyond the HPC market (not large enough)
 - Address the needs of European Industry **→** Car manufacturing market

EPI Vision

- Develop (and sell) an EU-made family of High-Performance Processors for:
 - High Performance Computers
 - Connected mobility & AD Autonomous (Driving computing needs beyond 2023)
 - Other markets under exploration (Server, Cloud)
- Leveraging technical synergies between the markets and aggregate financial efforts across these markets







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EPI Consortium

EPI 23 partners, from research to industry





EPI Common Platform (gen1)



EPI Common Platform Scalability





EPI view of ExaScale processors

- As an ExaScale processor
 - Specialization is the only way toward energy efficiency
 - Bytes/flops has to be improved for new HPC workloads
- As a consequence for processor implementation in EPI:
 - Use/Design specific computing units (ARM/SVE + EPAC + MPPA + ..)
 - Ease heterogeneous integration of above computing units thanks to a common design platform at SoC level and package level.
 - Put as much as possible large amount of memory close to the processing units (HBM)
 - Adapt the NoC and Die-2-Die BW requirements to the use of HBM with so many heterogeneous processing units





EPI Streams

S1 - Common Stream

S2 - GPP Processor

S3 - Acceleration

S4 - Automotive

S5 - Administration

Codesign, Architecture, System software and key technologies for the Common Platform

> Design and implement of the processor chip(s) and PoC system

Foster acceleration technologies and create building blocks

Address automotive market needs and create a pilot eHPC system

Manage and support activities

EPI Co-design

Software Support

- EPI will supply the full software stack for the processor, from reference firmware and UEFI to end-user tools compilers, libraries, runtimes, tools
 - Enabling direct use of the design
 - Enabling integration of EPI technology in derived designs
- Tools are developed in partnership between the project partners such as Atos and BSC and the ecosystem partners such as Arm and Linaro
 - Leverage ecosystem efforts & previous projects such as Mont-Blanc
 - Develop tools to fully support EPI specificities such as embedded accelerators, HBM or secure subsystem
- Major scientific codes are used as the basis for the co-design of the processor and accelerators
 - Ensure that the final design suits supercomputing needs
- Industrial partners supply the first reference platforms along with a full software environment for HPC & eHPC

EPI Software Infrastructure

* for simplification, only WP leaders and major components are listed.

With EPI, Europe has the ambition to repeat the Airbus success

20's Century

21's Century

